CLAIMS

What is claimed is:

1. A fabrication method for a non-volatile memory device, said method comprising:

providing a semiconductor substrate comprising a dielectric layer formed on thereon, an insulating composite layer formed on said dielectric layer;

forming a patterned protective patterning layer and a patterned first sacrificial layer on said insulating composite layer;

trimming said protective patterning layer;

patterning said first sacrificial layer by using said protective patterning layer as masks, wherein said first sacrificial layer comprises an opening that exposes said insulating composite layer;

removing said protective patterning layer;

filling a second sacrificial layer in said opening of said first sacrificial layer;

patterning said first sacrificial layer and said insulating composite layer by using said second sacrificial layer as masks and exposing said dielectric layer;

removing said second sacrificial layer; and

forming a control gate on said composite layer.

2. The method according to claim 1, wherein said dielectric layer is a silicon dioxide layer.

3. The method according to claim 1, wherein said insulating composite layer is formed of a silicon dioxide layer and a silicon nitride layer.

4. The method according to claim 1, wherein said first sacrificial layer a polysilicon layer.

5. The method according to claim 1, wherein said second sacrificial layer is a silicon nitride layer.

6. The method according to claim 1, wherein said control gate is a polysilicon gate.

7. The method according to claim 1, wherein said protective patterning layer is a photoresist layer.

8. A method for making a twin bit cell memory device, comprising the steps of:

forming on a substrate a tunnel dielectric layer, an insulating charge-trapping layer overlying the tunnel dielectric layer, and a second dielectric layer overlying the charge-trapping layer;

forming on said substrate a first patterned sacrificial material overlying said second dielectric layer;

using at least said first patterned sacrificial material as a mask, introducing impurities into said substrate;

filling openings in said first patterned sacrificial material with a second sacrificial material;

removing said first patterned sacrificial material to expose portions of said second dielectric layer through said second sacrificial material;

using said second sacrificial material as a mask, opening through-holes in said exposed portions of said second dielectric layer and portions of said charge-trapping layer underlying said exposed portions of said second dielectric layer;

removing said second sacrificial material; and

forming control gates overlying said second dielectric layer and extending over said through-holes.

9. A method according to claim 8, further comprising the step of widening said openings in said first patterned sacrificial material after said step of introducing impurities and before said step of filling openings in said first patterned sacrificial material.

10. A method according to claim 9, wherein said first patterned sacrificial material comprises a first sublayer of sacrificial material and a photoresist superposing said first sublayer of sacrificial material, and wherein said step of widening said openings comprises the steps of:

trimming said photoresist; and

using said photoresist as a mask, re-patterning said first sublayer of sacrificial material.

11. A method according to claim 8, wherein said control gates formed in said step of forming control gates also fill said through-holes.

12. A method according to claim 8, wherein said tunnel dielectric layer comprises silicon dioxide.

13. A method according to claim 8, wherein said second dielectric layer comprises silicon dioxide and said charge-trapping layer comprises silicon nitride.

14. A method according to claim 8, wherein said first sacrificial material comprises polysilicon.

15. A method according to claim 8, wherein said second sacrificial material comprises silicon nitride.

16. A method according to claim 8, wherein said control gates comprise polysilicon.